



Figure 1

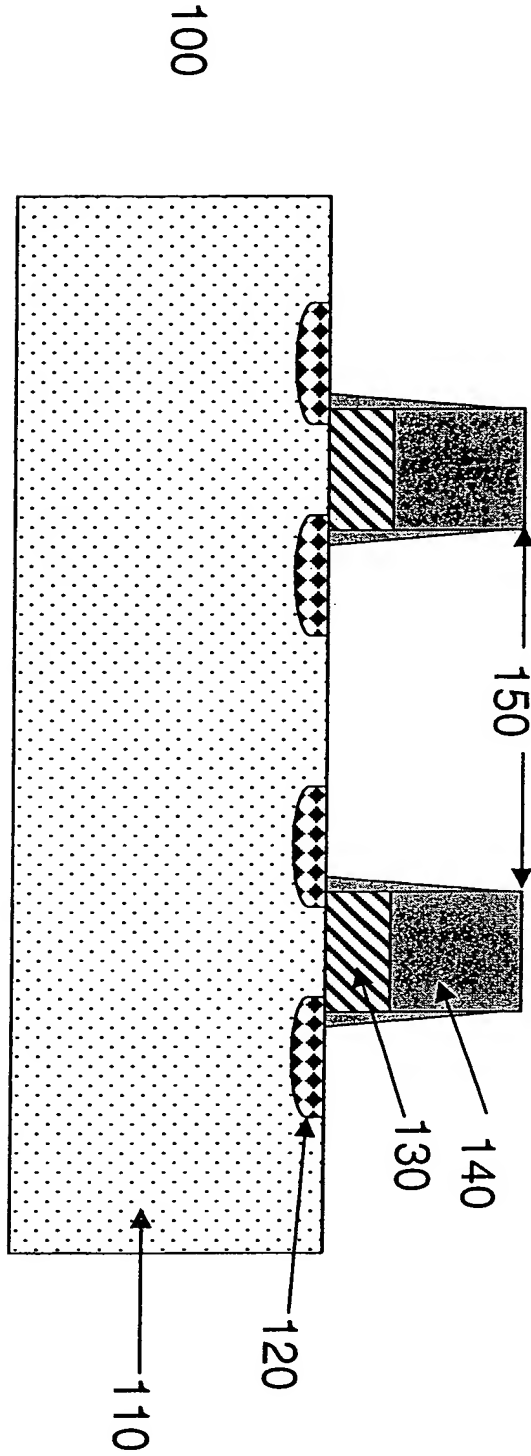


Figure 2

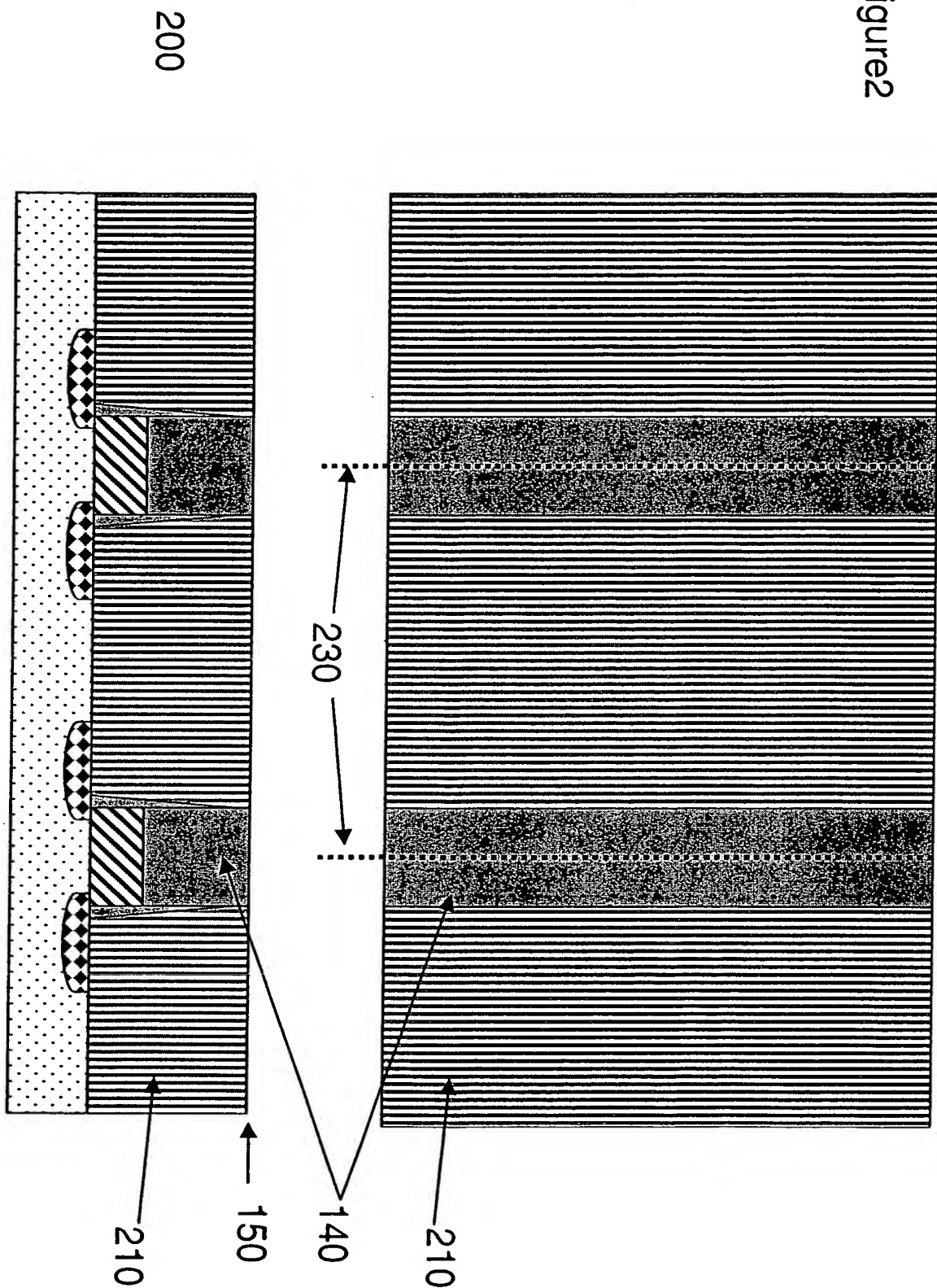


Figure 3

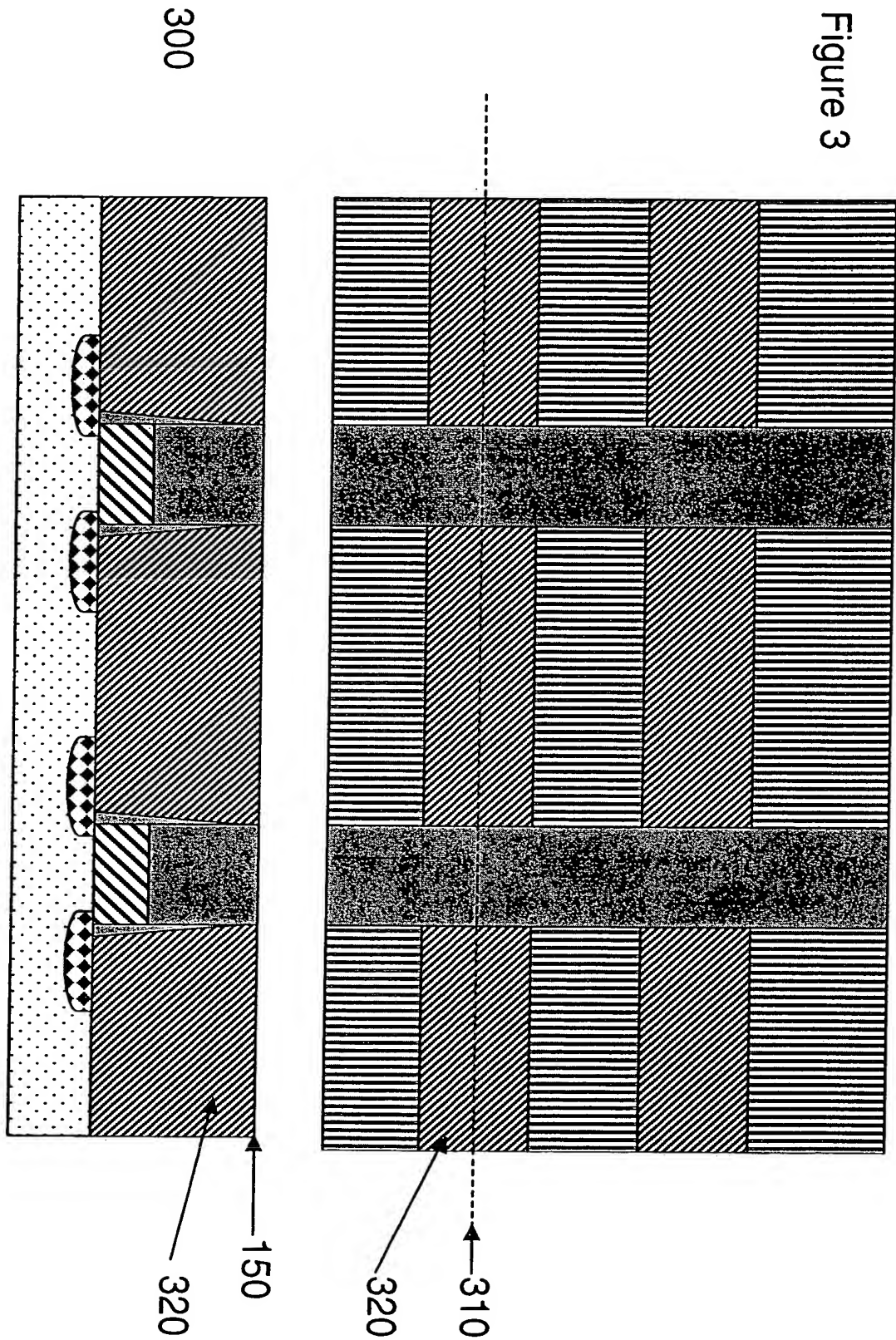


Figure 4

400

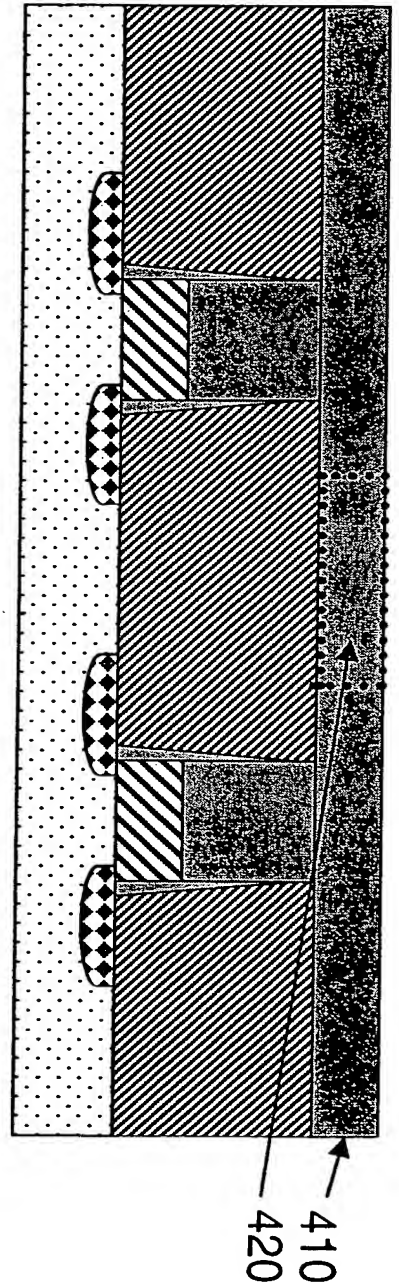


Figure 5

500

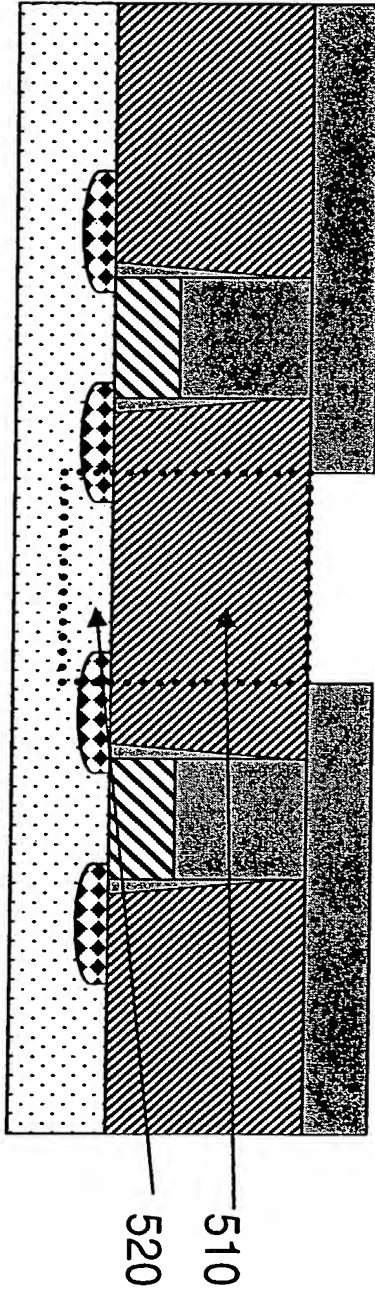


Figure 6

600

640

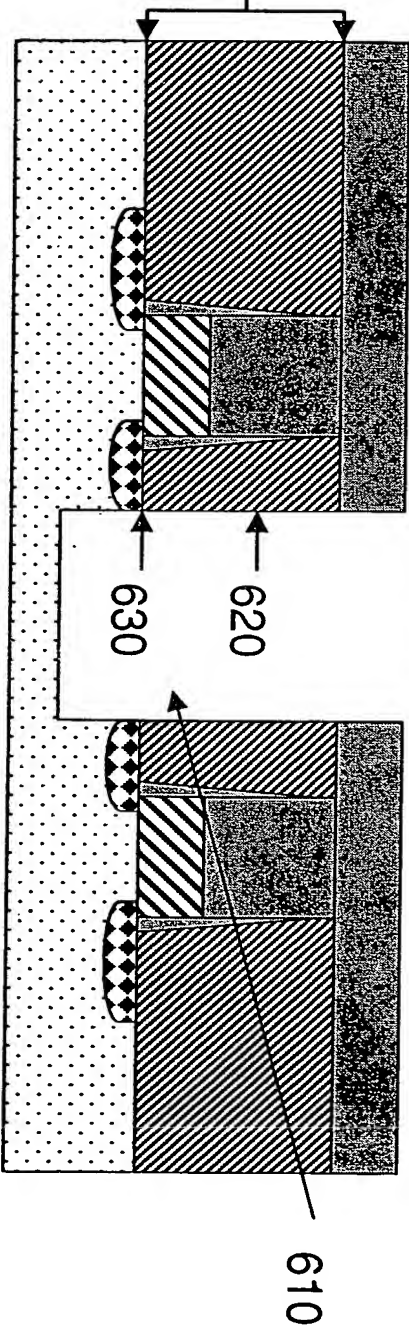


Figure 6A

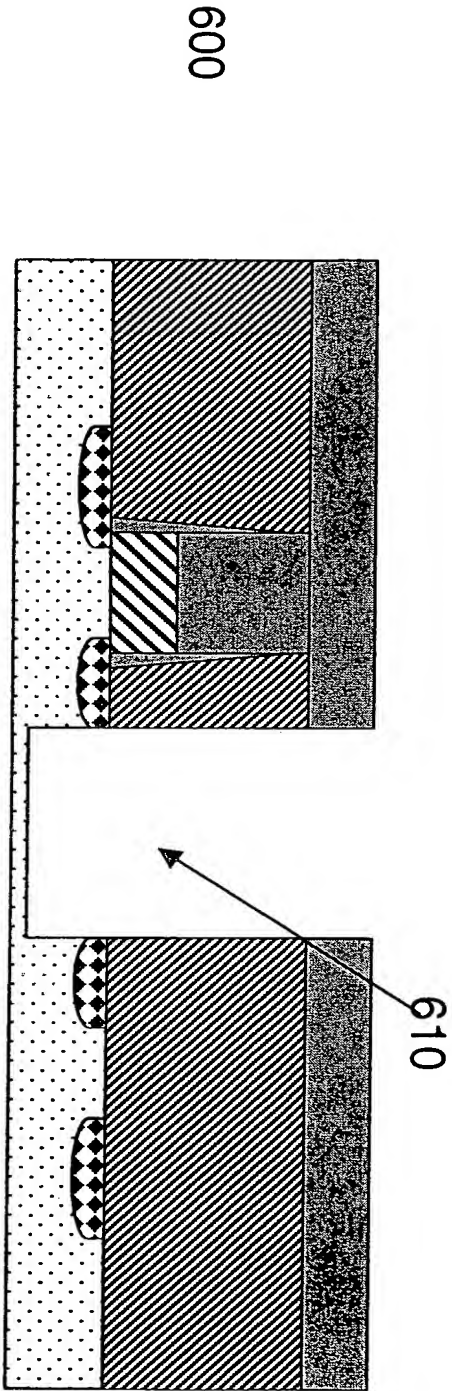


Figure 7

700

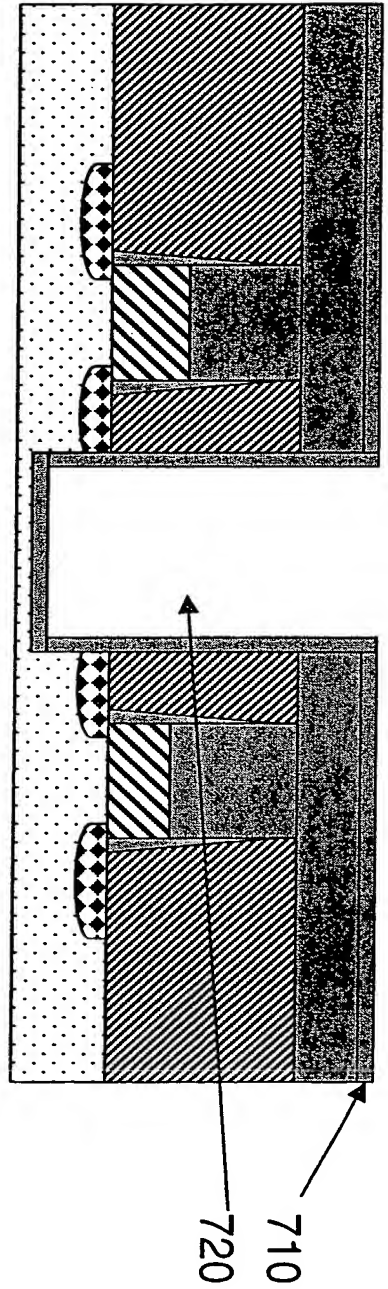


Figure 8

800

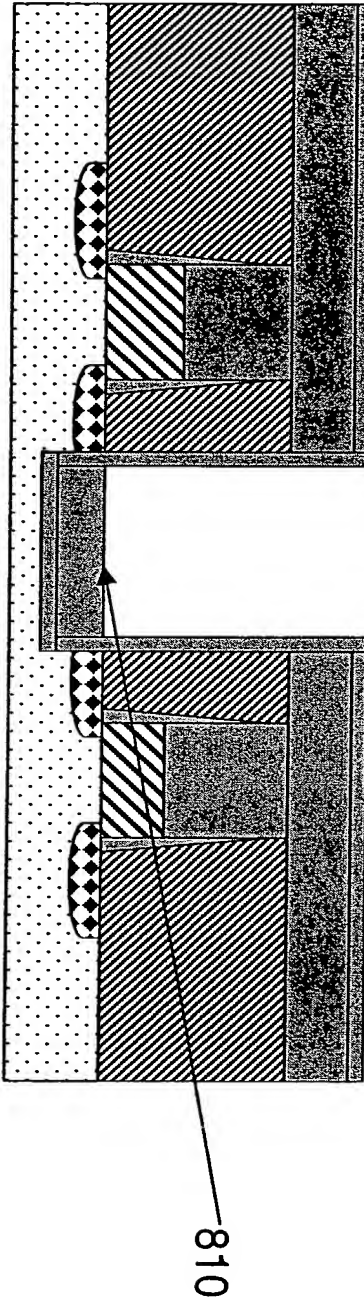


Figure 9

900

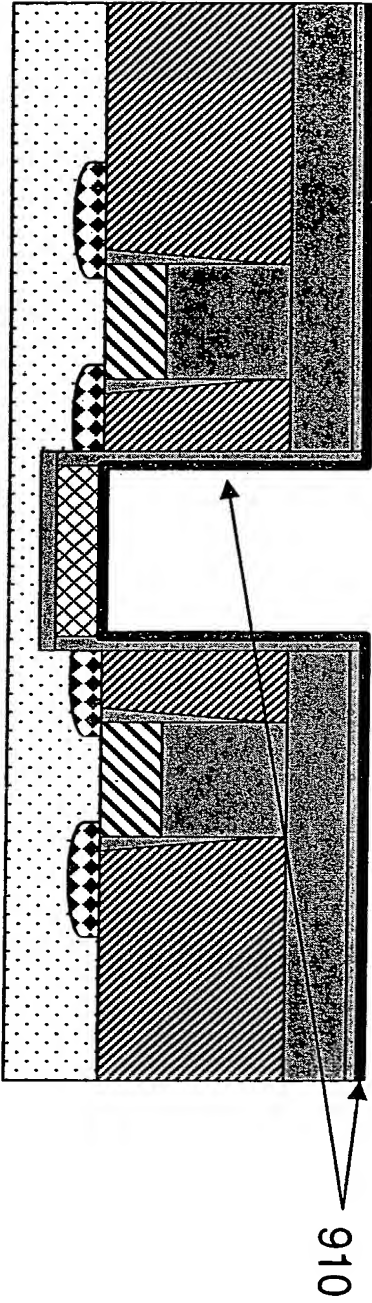


Figure 10

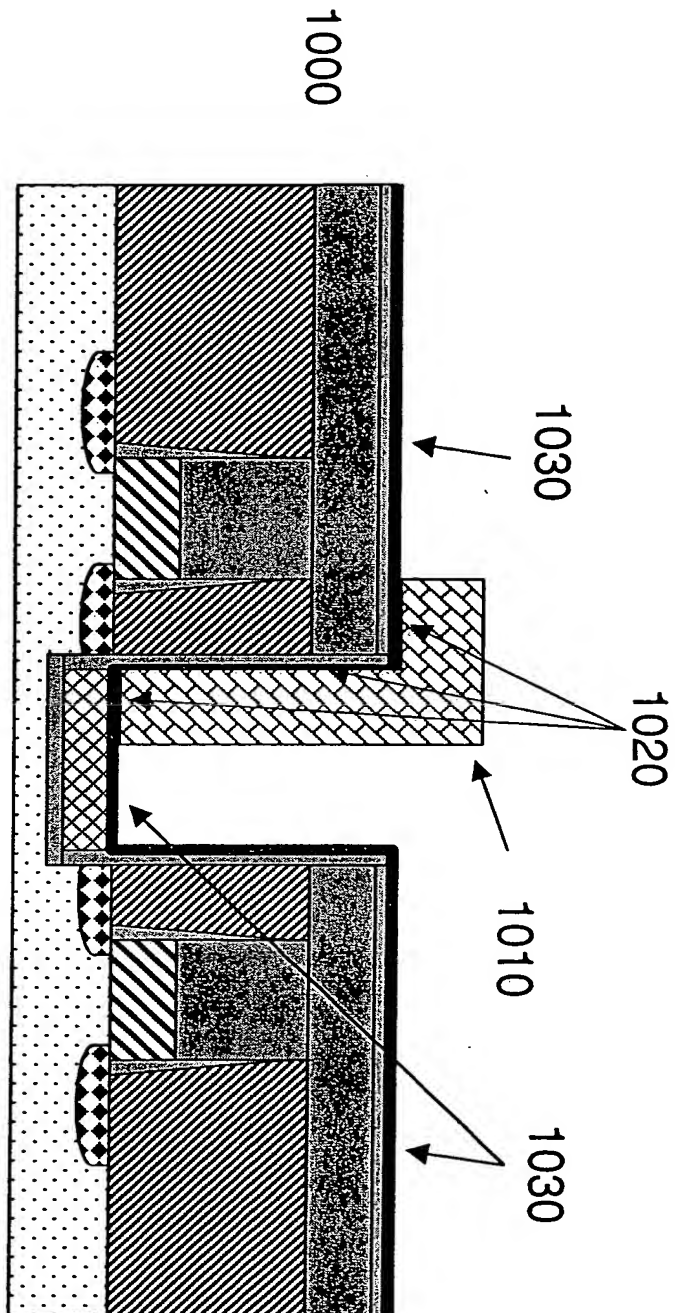


Figure 11

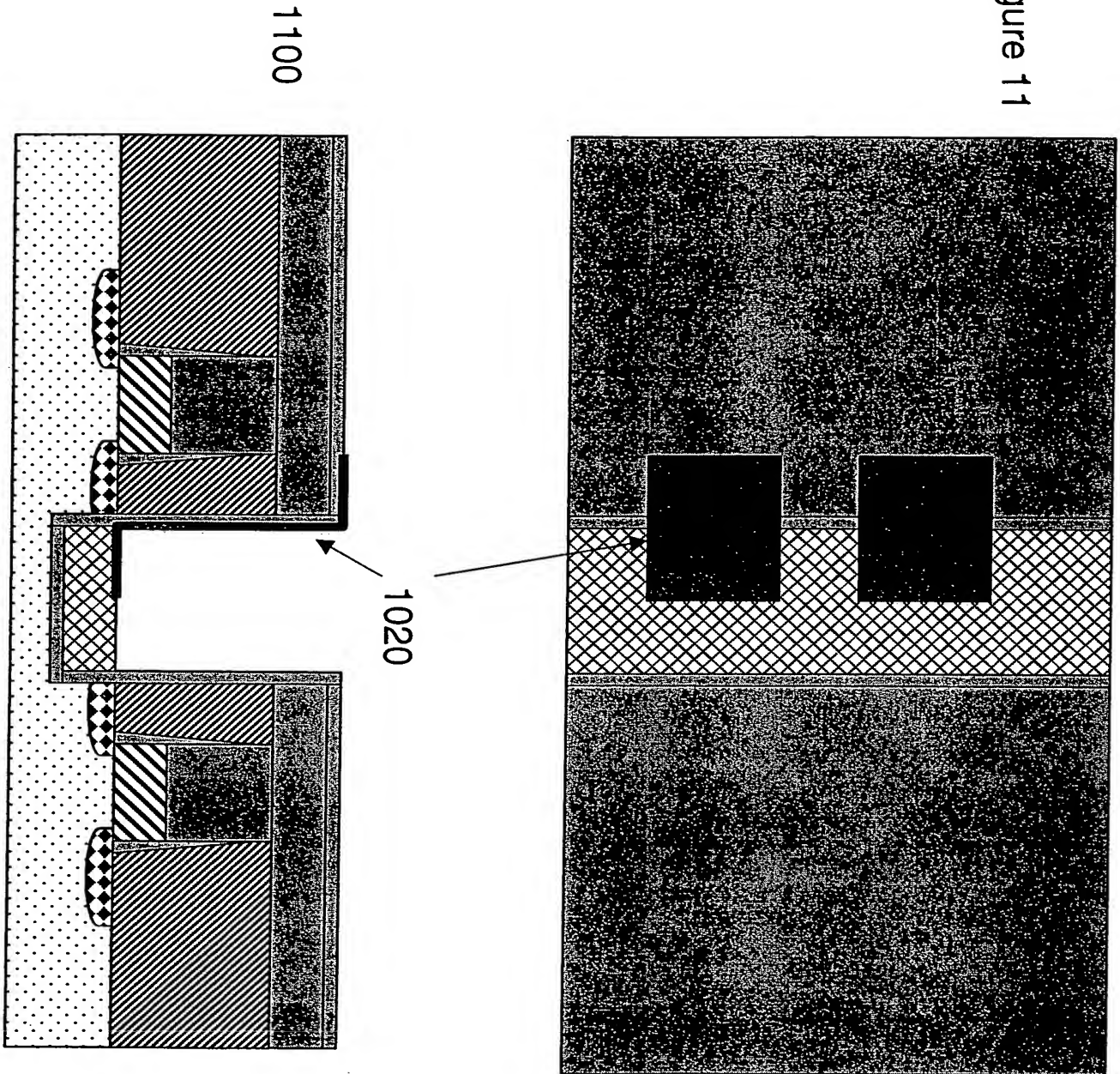


Figure 12

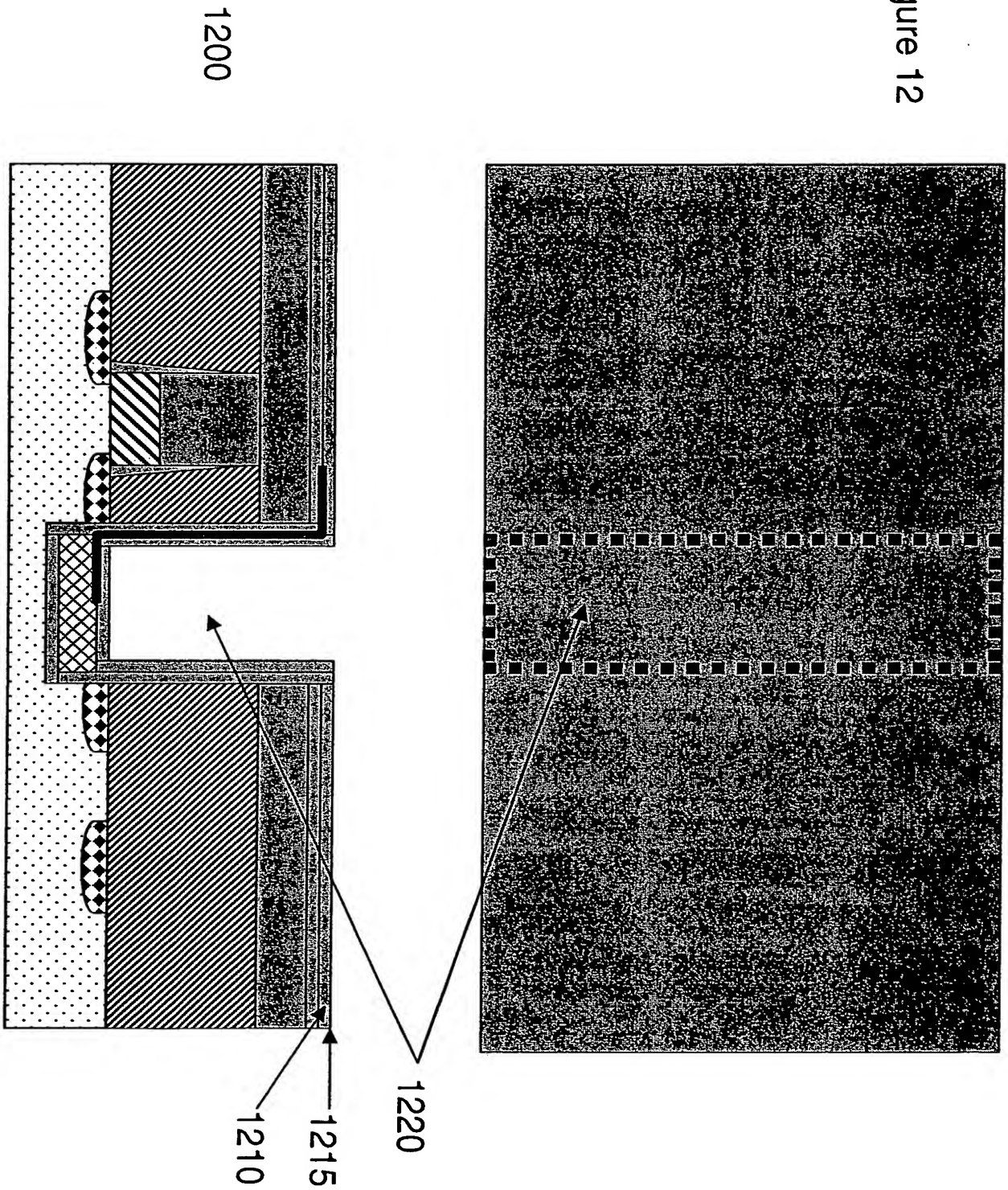


Figure 13

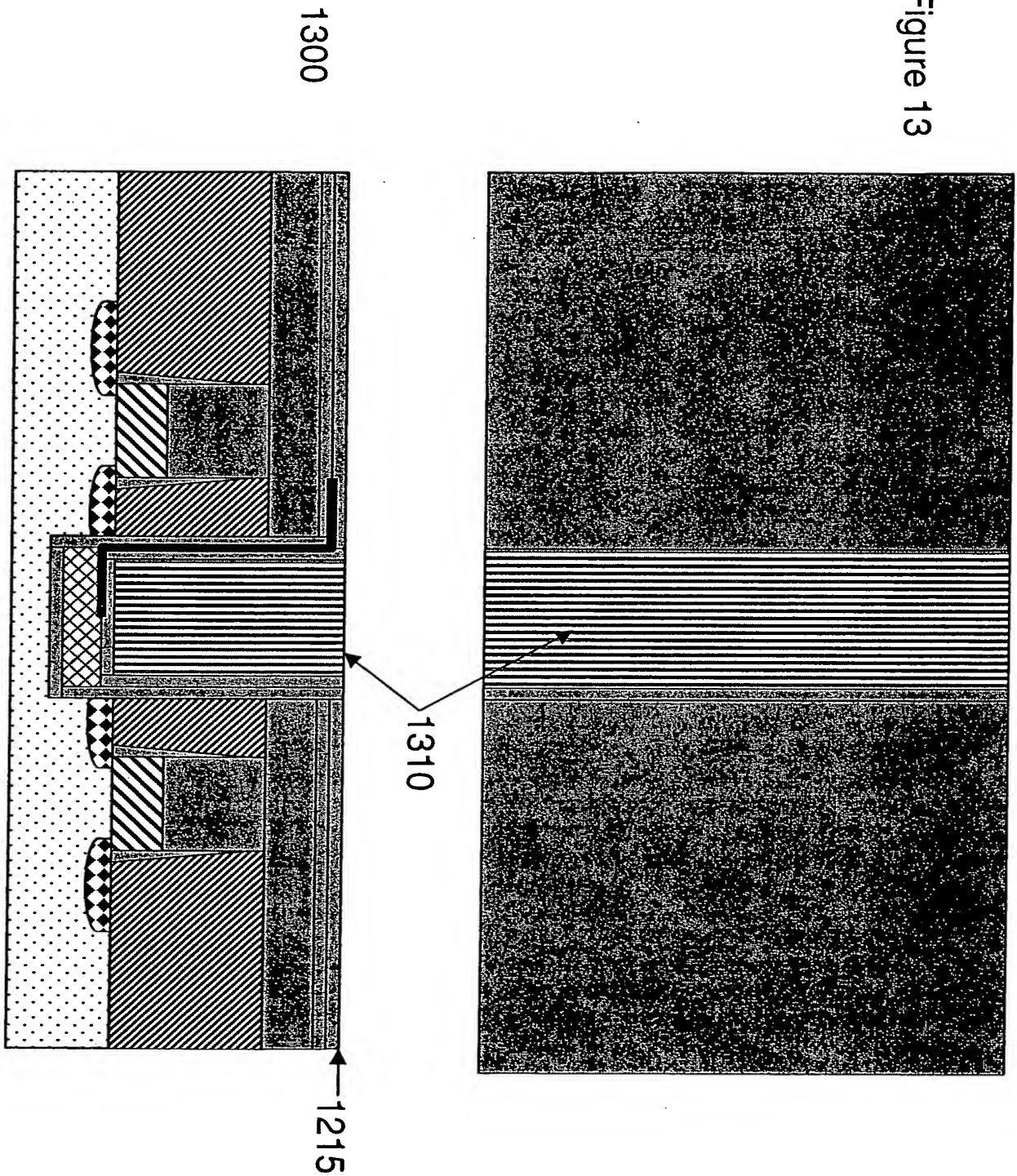


Figure 14

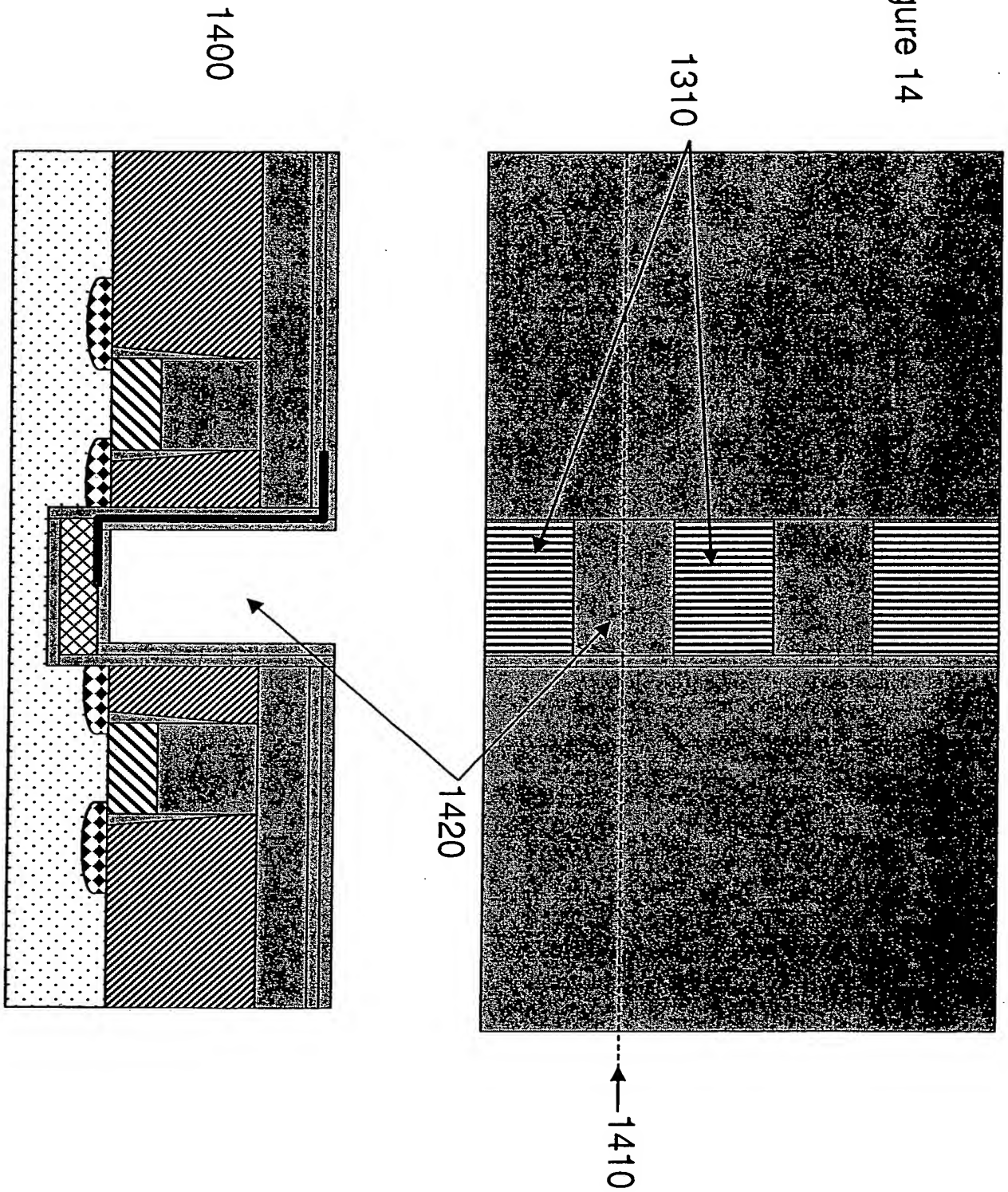


Figure 15

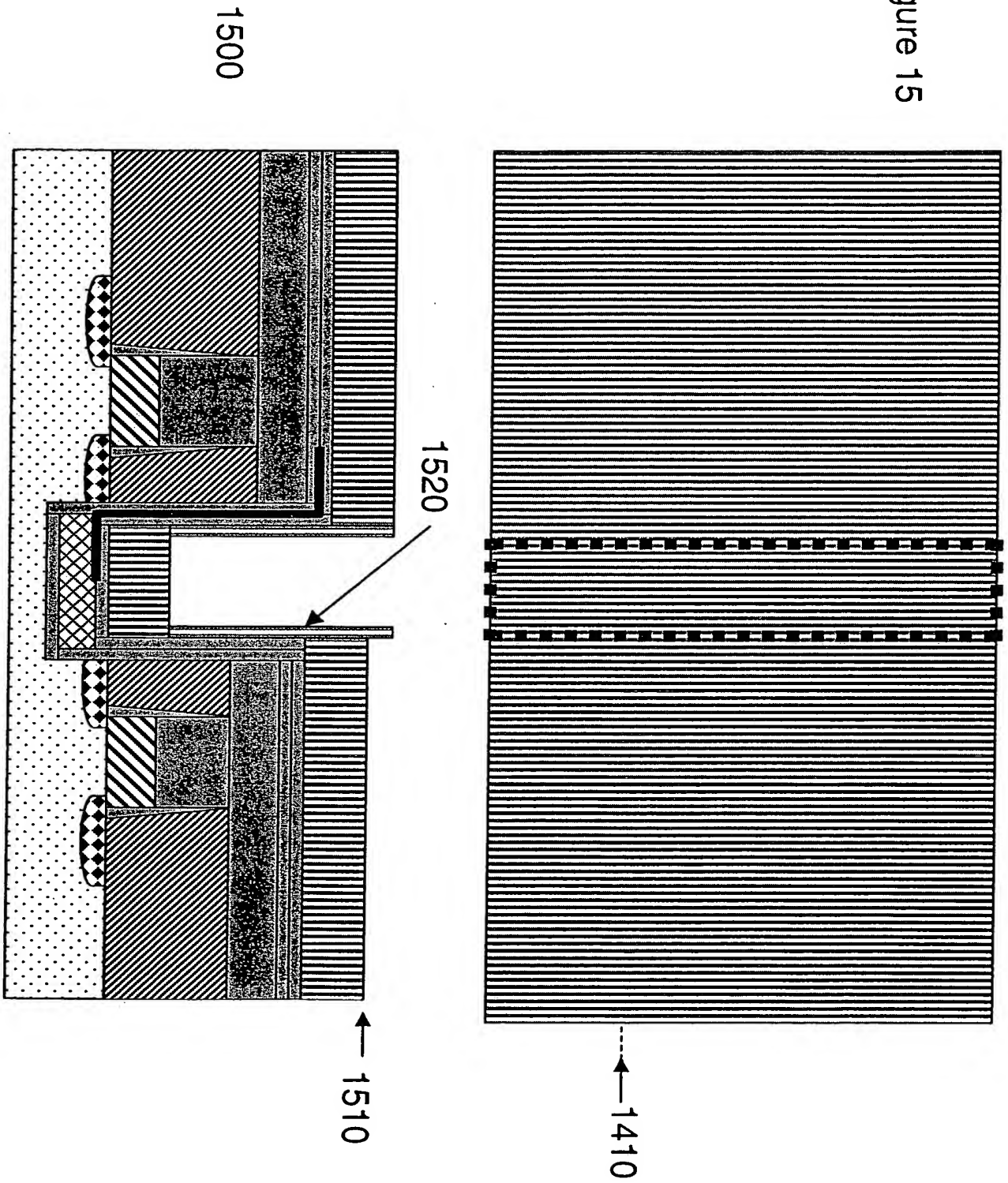


Figure 16

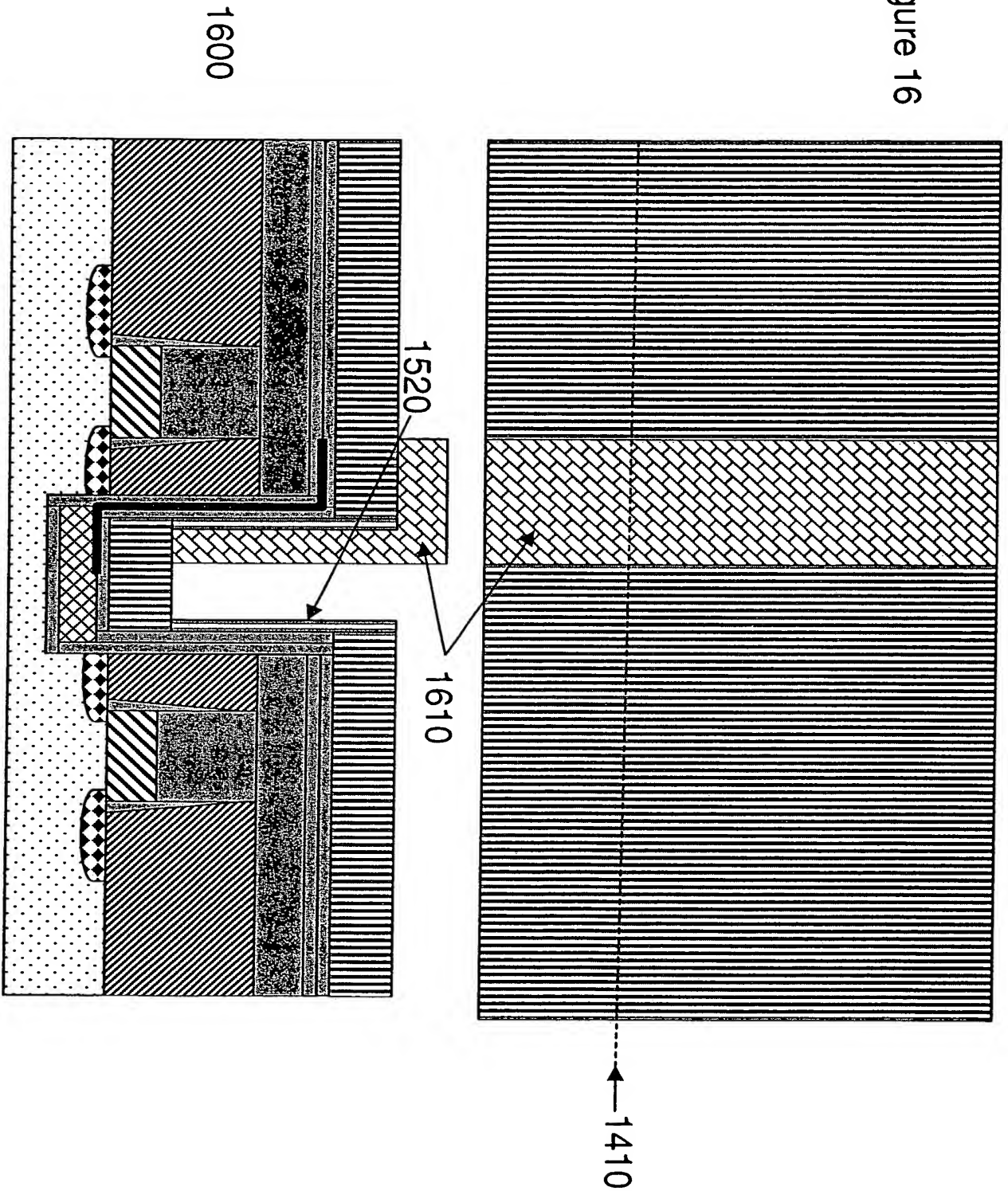


Figure 17

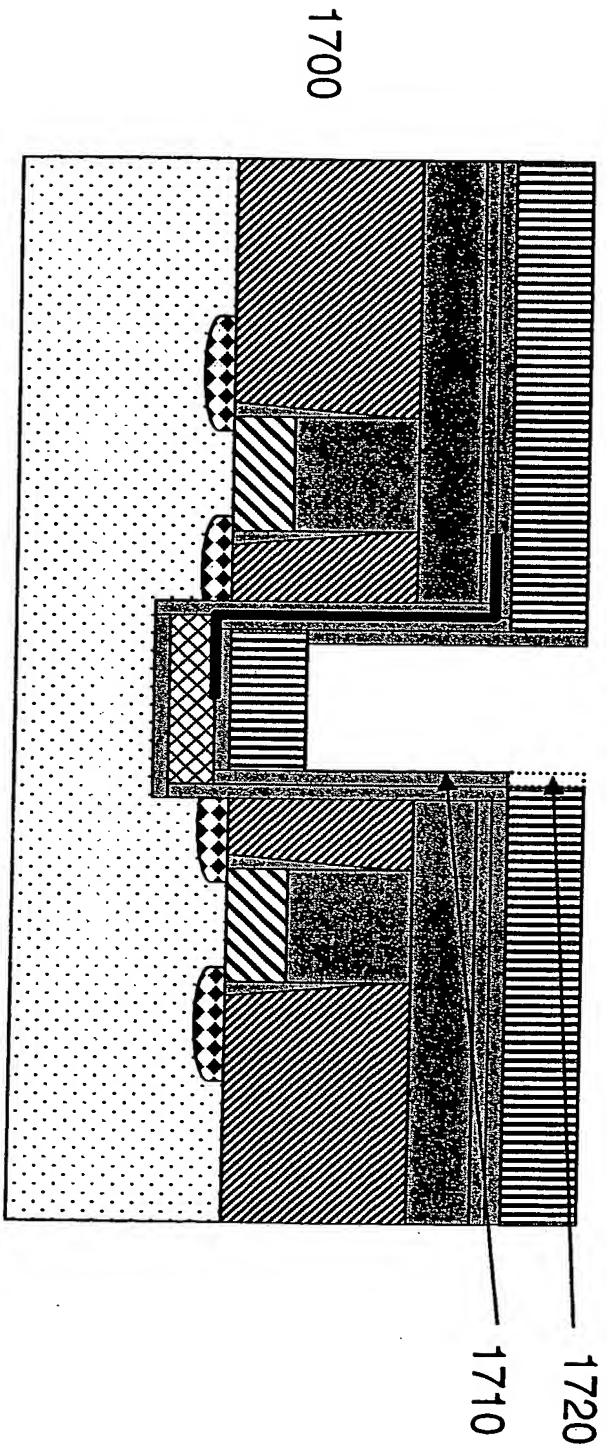
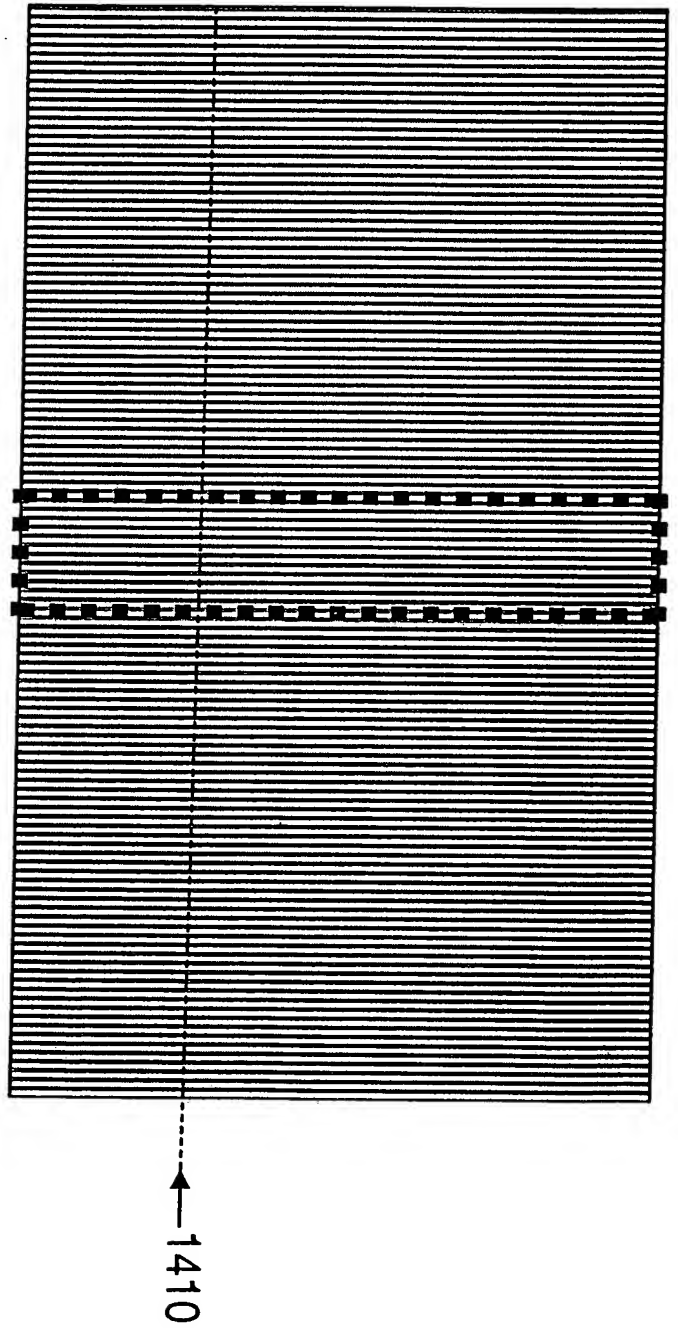


Figure 18

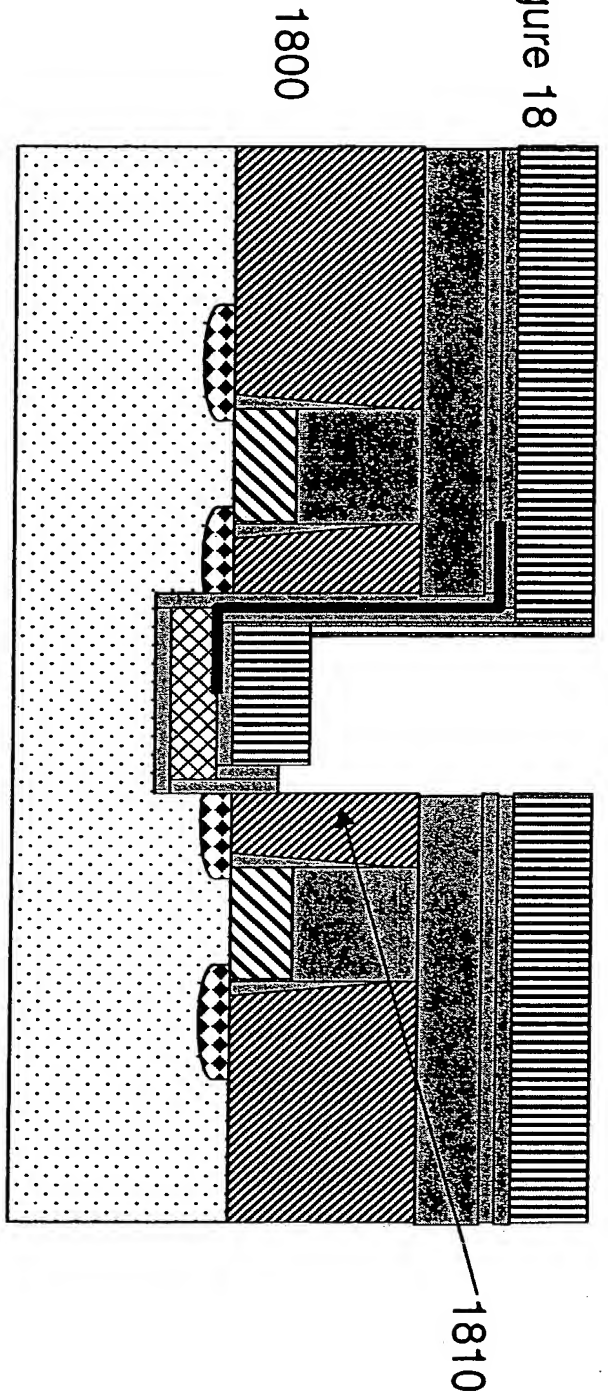


Figure 19

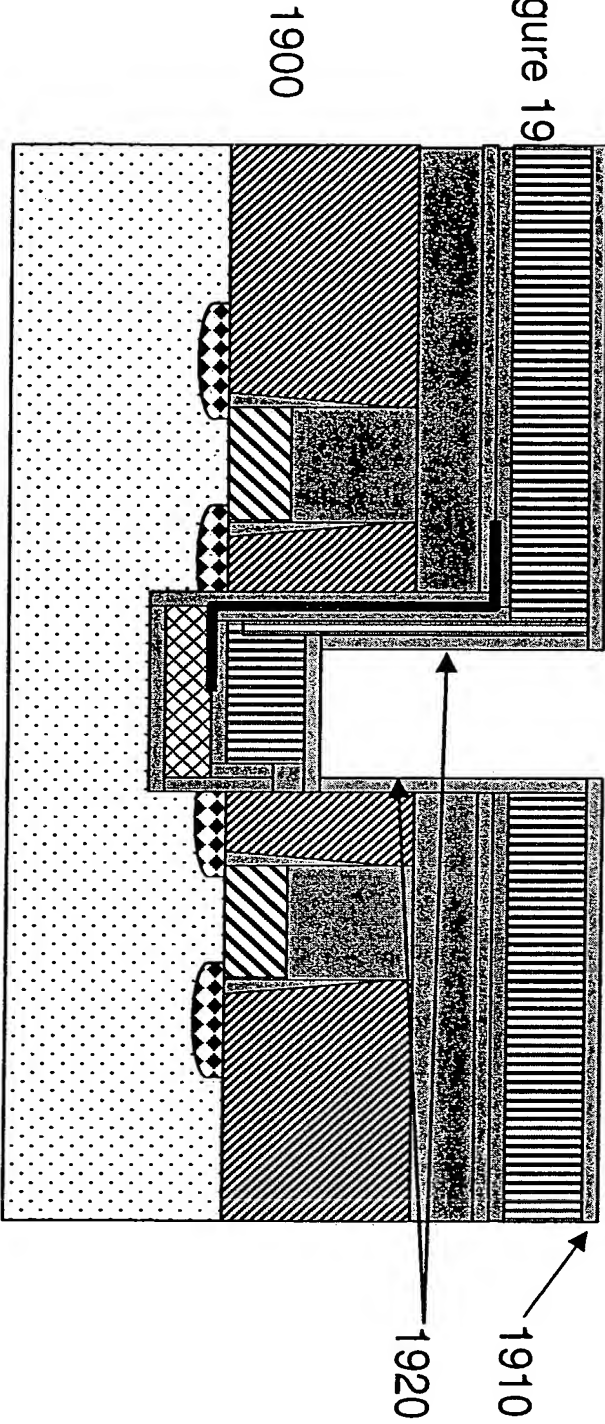


Figure 20

2000

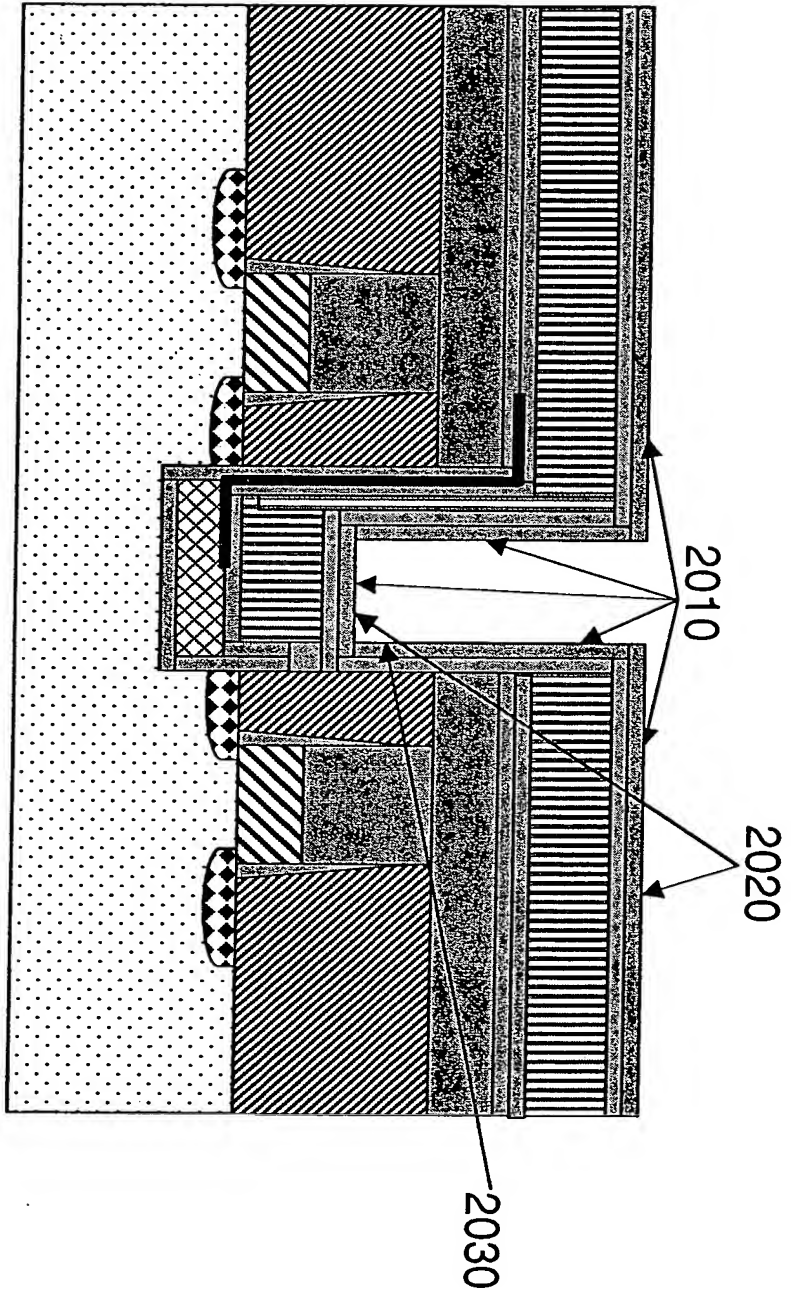


Figure 21

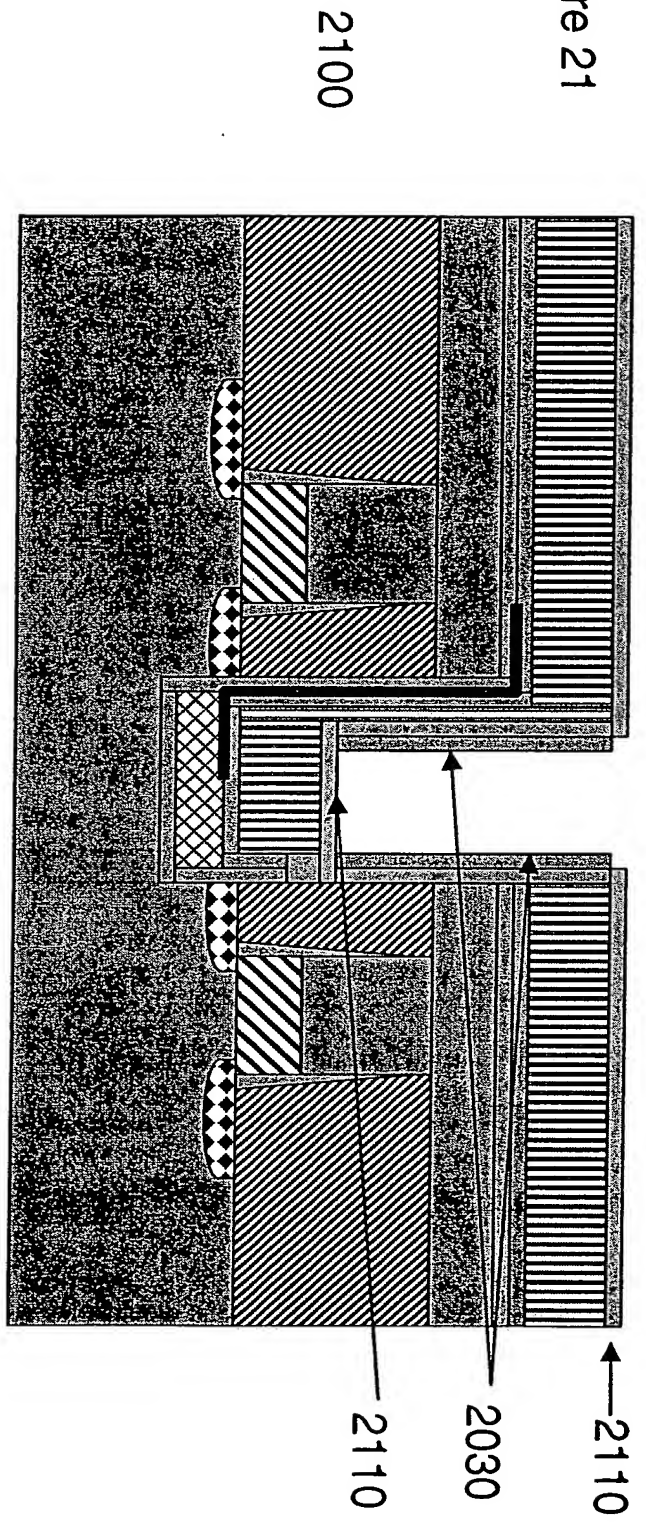


Figure 22

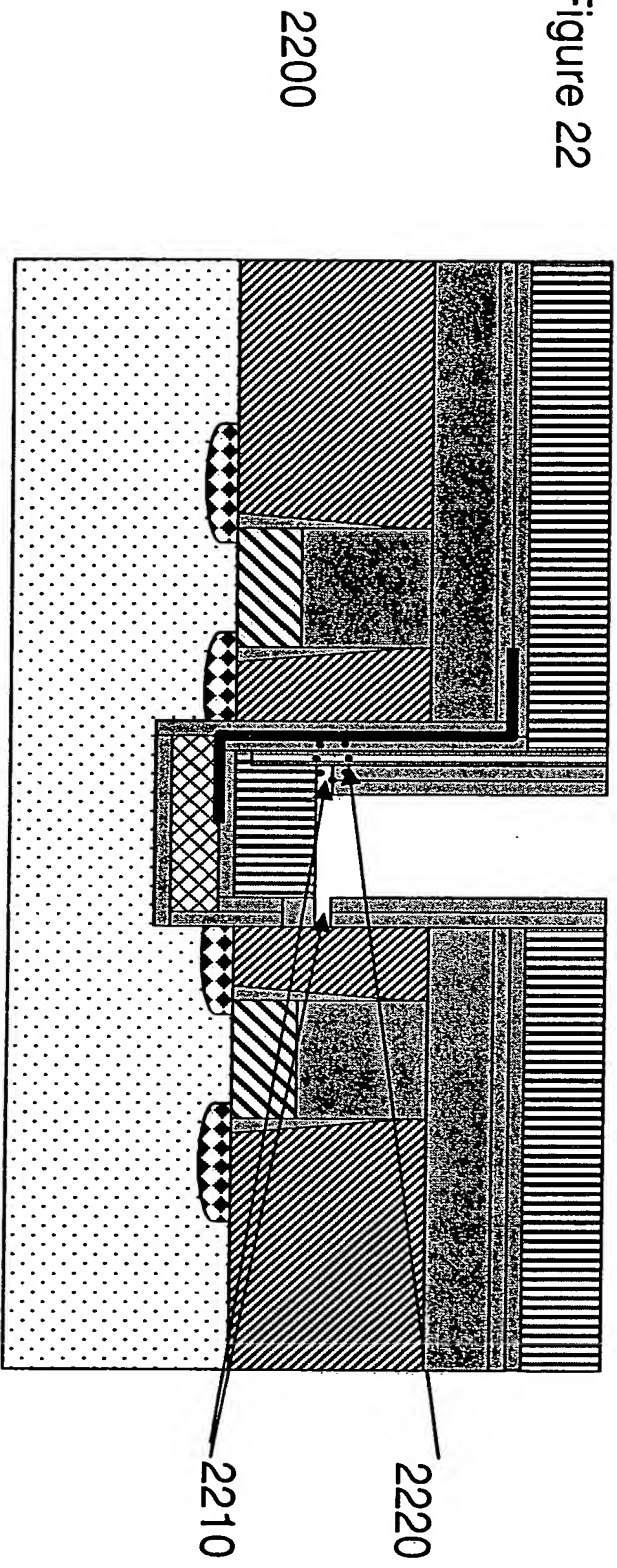
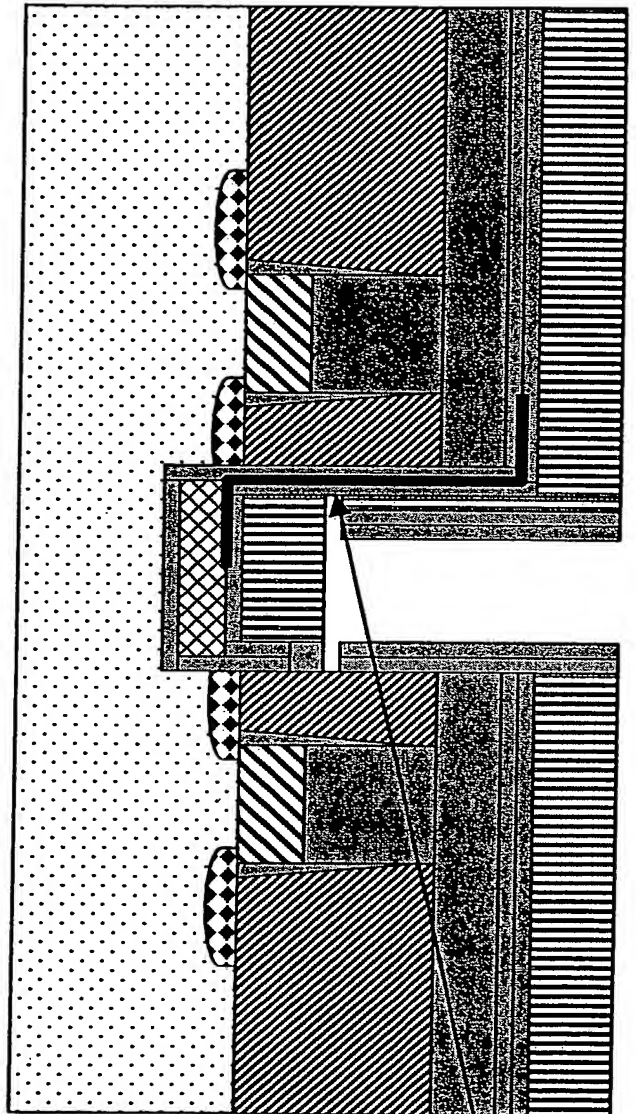


Figure 23

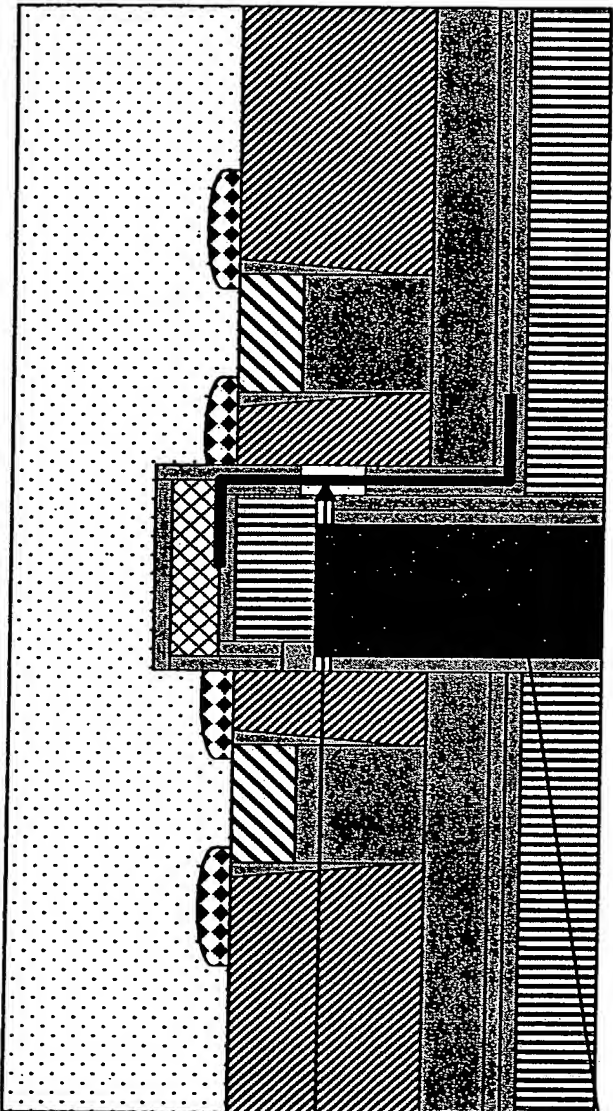
2300



2310

Figure 24

2400



2420

2410

Figure 25

Bit erasable 12 F² cell layout

